IN THE CLAIMS

Please amend the claims as follows:

1. A semiconductor device comprising:

a buffer semiconductor layer made of $Al_{1-s-t}Ga_sIn_tN$ ($0 \leq s \leq 1$, $0 \leq t \leq 1$, $s+t \leq 1$) and having a number of pinholes formed therein;

a thermal distortion reducing layer made of $Al_{1-u-v}Ga_uIn_vN$ ($0 \leq u \leq 1$, $0 < v \leq 1$, $u+v \leq 1$) formed on said buffer semiconductor layer and having a different chemical formula from that of said buffer semiconductor layer;

a first cladding layer formed on said thermal distortion reducing layer;

an active layer formed on said first cladding layer; and

a second cladding layer formed on said active layer.

2. The semiconductor device according to claim 1, wherein, in said $Al_{1-u-v}Ga_uIn_vN$ ($0 \leq u \leq 1$, $0 < v \leq 1$, $u+v \leq 1$) for said thermal distortion reducing layer, v is set to be not less than 0.1 and not more than 0.9.

3. A semiconductor device according to claim 1, wherein a film thickness of said thermal distortion reducing layer is greater than that of said semiconductor layer.

4. The semiconductor device according to claim 1, further comprising a cap layer on said thermal distortion reducing layer to prevent evaporation of In including in said thermal distortion reducing layer.

5. The semiconductor device according to claim 4, wherein said cap layer is made of $Al_{1-x}Ga_xN$ ($0 \leq x \leq 1$) and is formed at 500°C to 800°C.

6. The semiconductor device according to claim 1, wherein said first cladding layer is made of $Al_{1-x-y}Ga_xIn_yN$ ($0 \leq x \leq 1$, $0 \leq y \leq 1$, $x+y \leq 1$).

7. The semiconductor device according to claim 1, wherein said thermal distortion reducing layer has a thickness of 50 nm to 1000 nm.

8. A semiconductor device according to claim 1, further comprising a single crystal substrate on which said semiconductor layer is formed.

9. A semiconductor laser comprising:

a first layer;

a second layer made of $Al_{1-u-v}Ga_uIn_vN$ ($0 \leq u \leq 1$, $0 \leq v \leq 1$, $u+v \leq 1$) formed on said first layer,

a third layer formed on said second layer;

an active layer formed on said third layer; and

a fourth layer formed on said active layer,

wherein said first layer is formed of $Al_{1-s-t}Ga_sIn_tN$ ($0 \leq s \leq 1$, $0 \leq t \leq 1$, $s+t \leq 1$) with an average film thickness of 3 nm to 10 nm such that said first layer has a number of pinholes formed among said $Al_{1-s-t}Ga_sIn_tN$ ($0 \leq s \leq 1$, $0 \leq t \leq 1$, $s+t \leq 1$).

10. A semiconductor layer according to claim 9, further comprising a single crystal substrate on which said first layer is formed.

11. The semiconductor device according to claim 1, comprising:

a substrate;

said buffer semiconductor layer being formed on said substrate; and

said pinholes comprising exposed portions of said substrate through said buffer semiconductor layer.

12. The semiconductor device according to claim 1, wherein:

said buffer semiconductor layer comprises crystals formed spaced apart; and

said pinholes comprise spaces between said crystals.

13. The semiconductor device according to claim 1, wherein:

said buffer semiconductor layer comprises crystals loosely formed; and

said pinholes comprise spaces between said crystals.

14. The semiconductor device according to claim 1, wherein:

said buffer semiconductor layer consists essentially of an AlGaN material.

15. The semiconductor device according to claim 1, wherein:

said buffer semiconductor layer consists essentially of an AlN material.

16. A semiconductor device comprising:

a substrate;

crystals formed on said substrate and containing at least Al and N, said crystals being disposed so as to expose portions of said substrate;

a thermal distortion reducing layer made of $Al_{1-u-v}Ga_uIn_vN$ ($0 \leq u \leq 1$, $0 \leq v \leq 1$, $u+v \leq 1$) formed on said crystals and having a different chemical formula from that of said crystals;

a first cladding layer formed over said thermal distortion reducing layer;

an active layer formed over said first cladding layer; and

a second cladding layer formed over said active layer.

17. The semiconductor device according to claim 16, wherein:

said crystals consist essentially of an AlGaN material.

18. The semiconductor device according to claim 16, wherein:

said thermal distortion reducing layer consists essentially of a GaN material.

19. A semiconductor device comprising:

a substrate;

a buffer layer formed on said substrate and comprising a first layer made of $Al_{1-s-t}Ga_sIn_tN$ ($0 \leq s \leq 1$, $0 \leq t \leq 1$, $s+t \leq 1$) and a second layer made of $Al_{1-u-v}Ga_uIn_vN$ ($0 \leq u \leq 1$, $0 \leq v \leq 1$, $u+v \leq 1$) formed on said first layer and having a different chemical formula from that of said first layer;

a first cladding layer formed over said second layer;

an active layer formed over said first cladding layer; and

a second cladding layer formed over said active layer,

wherein said buffer layer comprises means for controlling polarity of a growth surface, said growth surface comprising at least a portion of a surface of said substrate.

20. A semiconductor device according to claim 19, wherein:

said means comprises pinholes.

21. A semiconductor device according to claim 19, wherein:

said means comprises a shape of said buffer layer.

22. The semiconductor device according to claim 19, further comprising:

a substrate wherein:

said buffer layer comprises crystals formed on said substrate; and

said means comprises intervals between said crystals exposing said substrate.

23. The semiconductor device according to claim 19, wherein:

said buffer layer consists essentially of an AlGaN material.

24. The semiconductor device according to claim 19, wherein:

said buffer layer consists essentially of an AlN material.

25. The semiconductor device of claim 19, wherein:

said thermal distortion reducing layer consists essentially of a GaN material.

26. A semiconductor device comprising:

a substrate;

a buffer layer formed on said substrate and made of $Al_{1-s-t}Ga_sIn_tN$ ($0 \le s \le 1$, $0 \le t \le 1$, $s+t \le 1$);

a thermal distortion reducing layer made of $Al_{1-u-v}Ga_uIn_vN$ ($0 \le u \le 1$, $0 \le v \le 1$, $u+v \le 1$) formed on said buffer layer and having a different chemical formula from that of said buffer layer;

a first cladding layer formed over said thermal distortion reducing layer;

an active layer formed over said first cladding layer; and

a second cladding layer formed over said active layer,

wherein said buffer layer comprises means for controlling polarity of a growth surface of said thermal distortion reducing layer, said growth surface comprising at least a portion of a surface of said substrate.

27. A semiconductor device according to claim 26, wherein:

said means comprises pinholes.

28. A semiconductor device according to claim 26, wherein:

said means comprises a shape of said buffer layer.

29. The semiconductor device according to claim 26, further comprising:

a substrate, wherein:

said buffer layer comprises crystals formed on said substrate; and

said means comprises intervals between said crystals exposing said substrate.

30. The semiconductor device according to claim 26, wherein:

said buffer layer consists essentially of an AlGaN material.

31. The semiconductor device according to claim 26, wherein:

said buffer layer consists essentially of an AlN material.

32. The semiconductor device of claim 26, wherein:

said thermal distortion reducing layer consists essentially of a GaN material.

33. A semiconductor device manufactured using a process comprising:

growing a first buffer layer of $Al_{1-s-t}Ga_sIn_tN$ ($0 \leq s \leq 1$, $0 \leq t \leq 1$, $s+t \leq 1$) on a surface of a substrate having portions exposing said surface of said substrate;

forming a second buffer layer of $Al_{1-u-v}Ga_uIn_vN$ ($0 \leq u \leq 1$, $0 \leq v \leq 1$, $u+v \leq 1$) on said first buffer layer and having a different chemical formula from that of said first buffer layer; and

forming an active layer over said second buffer layer.

34. A device according to claim 33, wherein said process comprises:

growing said first buffer layer at a temperature between 350° C and 800° C.

35. A device according to claim 33, wherein said process comprises:

forming said second buffer layer to absorb thermal distortion.

36. A device according to claim 33, wherein said process comprises:

forming said first buffer layer consisting essentially of A1GaN.

37. A device according to claim 33, wherein said process comprises:

forming said first buffer layer consisting essentially of A1N.

38. A device according to claim 33, wherein said process comprises:

forming said second buffer layer consisting essentially of GaN.

39. A device according to claim 33, wherein said process comprises:

forming said first buffer layer as spaced crystals.

40. A semiconductor device comprising:

a substrate;

crystals formed on said substrate and containing at least A1 and N, said crystals being loosely formed on said substrate;

a thermal distortion reducing layer made of $Al_{1-u-v}Ga_uIn_vN$ ($0 \leq u \leq 1$, $0 \leq v \leq 1$, $u+v \leq 1$) formed on said crystals and having a different chemical formula from that of said crystals;

a first cladding layer formed over said thermal distortion reducing layer;

an active layer formed on said first cladding layer; and

a second cladding layer formed on said active layer.

41. The semiconductor device according to claim 40, wherein said crystals consist essentially of an AlGaN material.

42. The semiconductor device according to claim 40, wherein said thermal distortion reducing layer consists essentially of a GaN material.

43. A semiconductor device comprising:

a substrate;

crystals formed on said substrate and containing at least Al and N, said crystals being formed spaced apart;

a thermal distortion reducing layer made of $Al_{1-u-v}Ga_uIn_vN$ ($0 \leq u \leq 1$, $0 \leq v \leq 1$, $u+v \leq 1$) formed on said crystals and having a different chemical formula from that of said crystals;

a first cladding layer formed over said thermal distortion reducing layer;

an active layer formed on said first cladding layer; and

a second cladding layer formed on said active layer.

44. The semiconductor device according to claim 43, wherein said crystals consist essentially of an AlGaN material.

45. The semiconductor device according to claim 43, wherein said thermal distortion reducing layer consists essentially of a GaN material.

46. A semiconductor device comprising:

a substrate;

crystals formed on said substrate and containing at least A1 and N, said crystals having intervals therebetween so as to expose said substrate;

a thermal distortion reducing layer made of $A1_{1-u-v}Ga_uIn_vN$ ($0 \leq u \leq 1$, $0 \leq v \leq 1$, $u+v \leq 1$) formed on said crystals and having a different chemical formula from that of said crystals;

a first cladding layer formed over said thermal distortion reducing layer;

an active layer formed on said first cladding layer; and

a second cladding layer formed on said active layer.

47. The semiconductor device according to claim 46, wherein said crystals consist essentially of an A1GaN material.

48. The semiconductor device according to claim 46, wherein said thermal distortion reducing layer consists essentially of a GaN material.

49. A semiconductor device comprising:

a substrate;

a buffer layer comprising a first layer made of $Al_{1-s-t}Ga_sIn_tN$ ($0 \leq s \leq 1$, $0 \leq t \leq 1$, $s+t \leq 1$) formed on said substrate;

a second layer made of $Al_{1-u-v}Ga_uIn_vN$ ($0 \leq u \leq 1$, $0 \leq v \leq 1$, $u+v \leq 1$) formed on said first layer and having a different chemical formula from that of said first layer;

a first cladding layer formed over said second layer;

an active layer formed over said first cladding layer; and

a second cladding layer formed over said active layer,

wherein said first layer comprises pinholes.

50. The semiconductor device according to claim 49, wherein said first layer consists essentially of an AlGaN material, and said second layer consists essentially of a GaN material.

51. A semiconductor device comprising:

a substrate;

a buffer layer comprising a first layer made of $Al_{1-s-t}Ga_sIn_tN$ ($0 \leq s \leq 1$, $0 \leq t \leq 1$, $s+t \leq 1$) formed on said substrate, and a second layer made of $Al_{1-u-v}Ga_uIn_vN$ ($0 \leq u \leq 1$, $0 \leq v \leq 1$, $u+v \leq 1$) formed on said first layer and having a different chemical formula from that of said first layer;

a first cladding layer formed over said second layer;

an active layer formed over said first cladding layer; and

a second cladding layer formed over said active layer,

wherein said first layer comprises crystals formed on said substrate, said crystals comprising intervals therebetween exposing said substrate.

52. The semiconductor device according to claim 51, wherein said first layer consists essentially of an AlGaN material, and said second layer consists essentially of a GaN material.

53. A semiconductor device comprising:

a substrate;

a buffer layer comprising a first layer made of $Al_{1-s-t}Ga_sIn_tN$ ($0 \le s \le 1$, $0 \le t \le 1$, $s+t \le 1$) formed on said substrate, and a second layer made of $Al_{1-u-v}Ga_uIn_vN$ ($0 \le u \le 1$, $0 \le v \le 1$, $u+v \le 1$) formed on said first layer and having a different chemical formula from that of said first layer;

a first cladding layer formed over said second layer;

an active layer formed over said first cladding layer; and

a second cladding layer formed over said active layer,

wherein said first layer comprises crystals formed spaced apart.

54. The semiconductor device according to claim 53, wherein said first layer consists essentially of an AlGaN material, and said second layer consists essentially of a GaN material.

55. A semiconductor device comprising:

a substrate;

a buffer layer comprising a first layer made of $Al_{1-s-t}Ga_sIn_tN$ ($0 \le s \le 1$, $0 \le t \le 1$, $s+t \le 1$) formed on said substrate, and a second layer made of $Al_{1-u-v}Ga_uIn_vN$ ($0 \le u \le 1$, $0 \le v \le 1$, $u+v \le 1$) formed on said first layer and having a different chemical formula from that of said first layer;

a first cladding layer formed over said second layer;

an active layer formed on said first cladding layer; and

a second cladding layer formed on said active layer,

wherein said first layer comprises crystals disposed so as to expose portions of said substrate.

56. The semiconductor device according to claim 55, wherein said first layer consists essentially of an A1GaN material, and said second layer consists essentially of a GaN material.

57. A semiconductor device comprising:

a substrate;

a buffer layer comprising a first layer made of $Al_{1-s-t}Ga_sIn_tN$ ($0 \leq s \leq 1$, $0 \leq t \leq 1$, $s+t \leq 1$) formed on said substrate, and a second layer made of $Al_{1-u-v}Ga_uIn_vN$ ($0 \leq u \leq 1$, $0 \leq v \leq 1$, $u+v \leq 1$) formed on said first layer and having a different chemical formula from that of said first layer;

a first cladding layer formed over said second layer; and

an active layer formed over said first cladding layer; and

a second cladding layer formed over said active layer,

wherein said first layer comprises crystals loosely formed on said substrate.

58. The semiconductor device according to claim 57, wherein said first layer consists essentially of an A1GaN material, and said second layer consists essentially of a GaN material.

59. A semiconductor device comprising:

a substrate;

a buffer layer made of $Al_{1-s-t}Ga_sIn_tN$ ($0 \leq s \leq 1$, $0 \leq t \leq 1$, $s+t \leq 1$) formed on said substrate;

a thermal distortion reducing layer made of $A1_{1-u-v}Ga_uIn_vN$ ($0 \leq u \leq 1$, $0 \leq v \leq 1$, $u+v \leq 1$)

formed on said buffer layer and having a different chemical formula from that of said buffer layer;

a first cladding layer formed over said thermal distortion reducing layer;

an active layer formed over said first cladding layer; and

a second cladding layer formed over said active layer,

wherein said buffer layer comprises crystals formed on said substrate, said crystals having intervals therebetween so as to expose said substrate.

60. The semiconductor device according to claim 59, wherein

said buffer layer consists essentially of an AlGaN material, and

said thermal distortion reducing layer consists essentially of a GaN material.

61. A semiconductor device comprising:

a substrate;

a buffer layer made of $Al_{1-s-t}Ga_sIn_tN$ ($0 \leq s \leq 1$, $0 \leq t \leq 1$, $s+t \leq 1$) formed on said substrate;

a thermal distortion reducing layer made of $Al_{1-u-v}Ga_uIn_vN$ ($0 \leq u \leq 1$, $0 \leq v \leq 1$, $u+v \leq 1$) formed on said buffer layer and having a different chemical formula from that of said buffer layer;

a first cladding layer formed over said thermal distortion reducing layer;

an active layer formed on said first cladding layer; and

a second cladding layer formed on said active layer,

wherein said buffer layer comprises crystals formed spaced apart on said substrate.

62. The semiconductor device according to claim 61, wherein

said buffer layer consists essentially of an AlGaN material, and

said thermal distortion reducing layer consists essentially of a GaN material.

63. A semiconductor device comprising:

a substrate;

a buffer layer made of $Al_{1-s-t}Ga_sIn_tN$ ($0 \leq s \leq 1$, $0 \leq t \leq 1$, $s+t \leq 1$) formed on said substrate;

a thermal distortion reducing layer made of $Al_{1-u-v}Ga_uIn_vN$ ($0 \leq u \leq 1$, $0 \leq v \leq 1$, $u+v \leq 1$) formed on said buffer layer and having a different chemical formula from that of said buffer layer;

a first cladding layer formed over said thermal distortion reducing layer;

an active layer formed on said first cladding layer; and

a second cladding layer formed on said active layer,

wherein said buffer layer comprises crystals disposed so as to expose portions of said substrate.

64. The semiconductor device according to claim 63, wherein

said buffer layer consists essentially of an A1GaN material, and

said thermal distortion reducing layer consists essentially of a GaN material.

65. A semiconductor device comprising:

a substrate;

a buffer layer made of $Al_{1-s-t}Ga_sIn_tN$ ($0 \leq s \leq 1$, $0 \leq t \leq 1$, $s+t \leq 1$) formed on said substrate;

a thermal distortion reducing layer made of $Al_{1-u-v}Ga_uIn_vN$ ($0 \leq u \leq 1$, $0 \leq v \leq 1$, $u+v \leq 1$) formed on said buffer layer and having a different chemical formula from that of said buffer layer;

a first cladding layer formed over said thermal distortion reducing layer;

an active layer formed on said first cladding layer; and

a second cladding layer formed on said active layer,

wherein said buffer layer comprises crystals loosely formed on said substrate.

66. The semiconductor device according to claim 65, wherein said buffer layer consists essentially of an A1GaN material, and

said thermal distortion reducing layer consists essentially of a GaN material.

67. A semiconductor device comprising:

a substrate;

crystals formed on said substrate and containing at least A1 and N;

a thermal distortion reducing layer made of $A1_{1-u-v}Ga_uIn_vN$ ($0 \leq u \leq 1$, $0 \leq v \leq 1$, $u+v \leq 1$) formed to contact said crystals and said substrate and having a different chemical formula from that of said crystals;

a first cladding layer formed over said thermal distortion reducing layer;

an active layer formed over said first cladding layer; and

a second cladding layer formed over said active layer.

68. The semiconductor device according to claim 67, comprising:

said thermal distortion reducing layer contacting said substrate through intervals between crystals.

69. A semiconductor device comprising:

a substrate;

a buffer layer comprising a first layer made of $Al_{1-s-t}Ga_sIn_tN$ ($0 \leq s \leq 1$, $0 \leq t \leq 1$, $s+t \leq 1$) formed on said substrate and a second layer made of $Al_{1-u-v}Ga_uIn_vN$ ($0 \leq u \leq 1$, $0 \leq v \leq 1$, $u+v \leq 1$) formed to contact said first layer and said substrate and having a different chemical formula from that of said first layer;

a first cladding layer formed over said second layer;

an active layer formed over said first cladding layer; and

a second cladding layer formed over said active layer.

70. The semiconductor device according to claim 69, comprising:

said second layer contacting said substrate through intervals in said first layer.

71. A semiconductor device comprising:

a buffer semiconductor layer made of $Al_{1-s-t}Ga_sIn_tN$ ($0 \leq s \leq 1$, $0 \leq t \leq 1$, $s+t \leq 1$) and having a number of pinholes formed therein;

a thermal distortion reducing layer made of $Al_{1-u-v}Ga_uIn_vN$ ($0 \leq u \leq 1$, $0 \leq v \leq 1$, $u+v \leq 1$) formed on said buffer semiconductor layer and having a different chemical formula from that of said buffer semiconductor layer;

a first cladding layer formed on said thermal distortion reducing layer;

an active layer formed on said first cladding layer; and

a second cladding layer formed on said active layer.

72. The semiconductor device according to claim 71, wherein, in said $Al_{1-u-v}Ga_uIn_vN$ ($0 \leq u \leq 1$, $0 \leq v \leq 1$, $u+v \leq 1$) for said thermal distortion reducing layer, v is set to be not less than 0.1 and not more than 0.9.

73. A semiconductor device according to claim 71, wherein a film thickness of said thermal distortion reducing layer is greater than that of said buffer semiconductor layer.

74. The semiconductor device according to claim 71, further comprising a cap layer on said thermal distortion reducing layer to prevent evaporation of In included in said thermal distortion reducing layer.

75. The semiconductor device according to claim 74, wherein said cap layer is made of $Al_{1-x}Ga_xN$ ($0 \leq x \leq 1$) and is formed at 500° C to 800° C.

76. The semiconductor device according to claim 71, wherein said first cladding layer is made of $Al_{1-x-y}Ga_xIn_yN$ ($0 \leq x \leq 1$, $0 \leq y \leq 1$, $x+y \leq 1$).

77. The semiconductor device according to claim 71, wherein said thermal distortion reducing layer has a thickness of 50 nm to 1000 nm.

78. A semiconductor device according to claim 71, further comprising a single crystal substrate on which said buffer semiconductor layer is formed.

79. The semiconductor device according to claim 71, comprising:

a substrate;

said buffer semiconductor layer being formed on said substrate; and

said pinholes comprising exposed portions of said substrate through said buffer semiconductor layer.

80. The semiconductor device according to claim 71, wherein:

said buffer semiconductor layer comprises crystals formed spaced apart; and

said pinholes comprise spaces between said crystals.

81. The semiconductor device according to claim 71, wherein:

said buffer semiconductor layer comprises crystals loosely formed; and

said pinholes comprise spaces between said crystals.

82. The semiconductor device according to claim 71, wherein:

said buffer semiconductor layer consists essentially of an AlGaN material.

83. The semiconductor device according to claim 71, wherein:

said buffer semiconductor layer consists essentially of an AlN material.

84. The semiconductor device according to claim 71, wherein:

said thermal distortion reducing layer consists essentially of a GaN material.

85. The semiconductor device of claim 71, comprising:

a substrate, said buffer semiconductor layer being formed on said substrate.

86. The semiconductor device according to claim 11, wherein:

said buffer semiconductor layer consists essentially of an AlGaN material.

87. The semiconductor device according to claim 11, wherein:

said buffer semiconductor layer consists essentially of an AlN material.

88. The semiconductor device according to claim 11, wherein:

said thermal distortion reducing layer consists essentially of a GaN material.

89. The semiconductor device of claim 12, comprising:

a substrate, said buffer semiconductor layer being formed on said substrate.

90. The semiconductor device of claim 13, comprising:

a substrate, said buffer semiconductor layer being formed on said substrate.